Development and Characterization of ac-coupled Si strip detectors for Nuclear & High Energy Physics Applications

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Introduction

Si detectors, in various configurations, have been playing an increasingly larger role in Nuclear and High Energy Physics (HEP) experiments.

The pixel and strip silicon detectors provide the best vertexing and tracking precision, and durability required for the physics studies. The aim of the present work was to design, develop and characterize ac-coupled, single side, p-in-n silicon strip detector in India as part of the R&D effort in collaboration with Bharat Electronics Limited (BEL), Bangalore and Fermilab/Argonne National Lab (ANL), USA for the future Nuclear and Particle physics experiments. The silicon detectors were fabricated at BEL on 4" wafers. Fermilab/ANL provided high-resistivity n-bulk silicon wafers, and the first detector design for this purpose. The design was optimized to produce detectors with high breakdown voltage and low leakage currents after extensive simulation studies using TCAD software. Further, the characterization facility is also developed at Delhi University to evaluate the basic performance of the fabricated detectors.

Design & Fabrication of Detectors

The initial detector design was chosen after reviewing designs of the detectors used at earlier experiments like D0 at Fermilab. Starting with the initial design, detailed simulation studies were performed using TCAD device simulator Silvaco [1] to optimize the detector process and device parameters. Optimization of breakdown voltage, interstrip capacitance, coupling capacitance etc. were performed by varying different parameters like junction depth, oxide thickness, guard ring spacing, guard ring width, strip width, strip pitch, metal overhang etc [2].

In the detector design, several test structures like MOS, pad diodes without and with different number of guard rings, gated diodes, mini strip detectors, etc. have been included. These structures provide basic understanding of the detectors and information of various parameters like flatband voltage, oxide charge density, full depletion voltage, interstrip resistance, interstrip capacitance, and coupling capacitance. This will help in tuning different parameters in simulations for the future design studies as well.

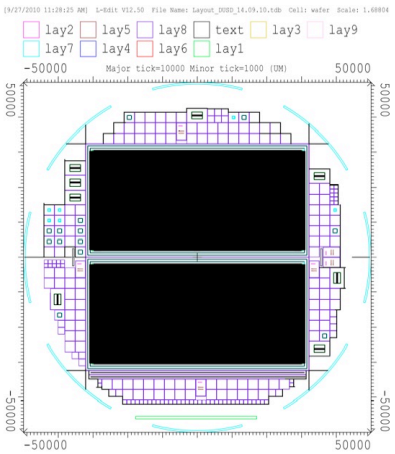

Fig. 1: Layer-wise mask image for detector development in kLayout software

Float-Zone n-bulk, 4" wafers with resistivity of 3-5 kohm-cm, thickness of 300 μm and orientation of <111> are used for fabrication. Each wafer contains two silicon strip detectors, each of which has a dimension of 6.43 cm × 3.25 cm. On the detector there are 512 p^+ strips with

strip width of 30 μm, strip pitch of 55 μm, and strip length of 6 cm. Four floating guard rings, each with an option to bias, are included in the design to reduce the leakage current and to increase the breakdown voltages of the strips. Metal overhang of 5 μm on individual strips are also used to increase the breakdown voltage as well. The bias ring is included to reverse bias the strips through the poly-silicon resistors. The detectors have been fabricated with eight-layer mask process using the planar fabrication technology. The fabricated detector layout is shown in Fig. 1. The coupling oxide thickness of 250 nm is used to achieve the desired coupling capacitance. The surface of the detectors is passivated with a silicon dioxide layer.

The desired specifications of low leakage currents, high coupling capacitance, low interstrip capacitance have been achieved by optimizing the process parameters such as ambient temperature and time for processes such as oxidation, implantation, annealing, drive-in, etc. A total of twelve detectors were fabricated.

Characterization of the Detectors

The basic operational characteristics, i.e. current-voltage (IV) and capacitance-voltage (CV) measurements have been performed on the fabricated detectors. A representative plot of IV measurement on the fabricated silicon strip detector is shown in Fig. 2. It can be seen that the detector has a leakage current of 20 μA at a reverse bias voltage of 300 V approximately, which meets the desired specifications.

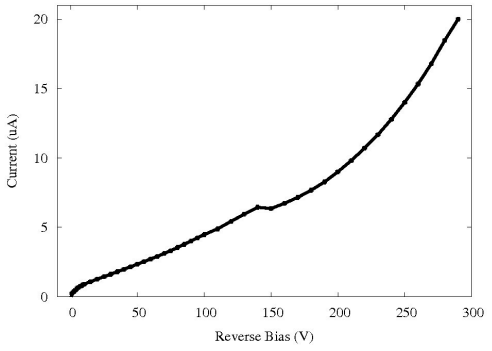

Fig. 2: IV measurement of one of the fabricated detectors.

Full depletion voltage and effective bulk density profile parameters can be obtained from the CV measurement, as shown in Fig. 3. The full depletion voltage is found to be approximately 85 V for the fabricated detector, which corresponds to bulk doping concentration of 1.2 x 10^{-12} cm^{-3}. This is consistent with the resistivity value of 3.5 kohm-cm.

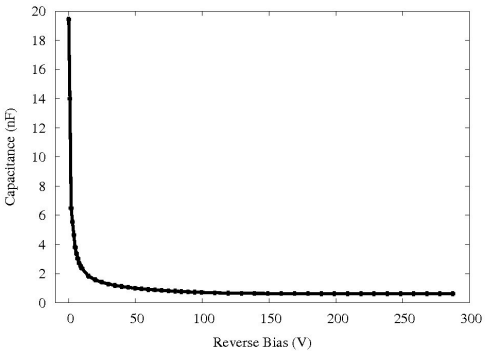

Fig. 3: CV measurement of one of the fabricated detectors.

In summary, the results on the fabricated detectors are encouraging and meeting the desired specification on IV and CV. Further measurements are still in progress on remaining silicon detectors and test structures.

Acknowledgement

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References

[1] ATLAS Silvaco version 5.15.32.R, Users manual, November 2009, http://www.silvaco.com..

[2] "Development of multi-guard ring-equipped p+–n Si microstrip sensors for the SiD detector at the ILC", P Saxena, K. Ranjan, A. Bhardwaj, R. K. Shivpuri and S Bhattacharya, Semicond. Sci. Technol. 25, 105012 (2010).