Performance of ANUSPARSH-III ASIC chipset with 1 m × 2 m glass RPC

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Introduction

India-based Neutrino Observatory (INO) is a mega science project of India which aims to build an underground observatory to study the properties of neutrinos. A major experiment to be housed in the observatory is a massive 50 kt magnetized Iron Calorimeter (ICAL) [1] detector. It would be employing about 30,000 square shaped RPCs of 2 m^2 area interleaved with iron plates. The ANUSPARSH ASIC chipset has been developed by the Electronics Division, BARC to be employed in frontend electronics of the ICAL to amplify and discriminate signals obtained from the RPCs. Tests were done at RPC lab, NPD-BARC to see the performance of the chipset with 2 m long copper readouts of the RPC.

1. 1 m × 2 m RPC

A 1 m × 2 m RPC was assembled at RPC lab, NPD-BARC using two square glass gaps of 1 m^2 area. Fig. 1(a) shows the RPC under assembly. The two gas gaps were connected using thermoformable U tubes so that the flow of the gas mixture (Freon R134a : 95.2%, *i*-butane : 4.5%, SF_6 : 0.3%) was common through both the gaps. These gaps were sandwiched between two 1 m × 2 m polycarbonate honeycomb copper readouts of 5 mm thickness, having 2 m long strips obtained from TIFR. This assembly was further sandwiched between aluminium honeycombs for support and the sides were covered by aluminium tapes to shield from EM interference. The width of the strips is ∼3 cm. The readout strips had 50 Ω termination at one end and the other end was soldered with 50 Ω coaxial cables having relimate connectors. Fig. 1(b) shows the assembled RPC. RPC was placed in the Hodoscope [2].

(a) RPC being assembled (b) The Assembled RPC

FIG. 1: The 1 m × 2 m glass RPC.

2. ANUSPARSH Frontend and DAQ

The ANUSPARSH-III ASIC chipset based RPC frontend board comprises of two ANUSPARSH-IIIA and one ANUSPARSH-IIID ASICs. The ANUSPARSH-IIIA ASIC is a four-channel, low power, fast voltage amplifier ASIC, providing a total channel gain of ∼70. Each frontend channel of ANUSPARSH-IIIA ASIC is comprised of three stages of differential amplifiers with independent common mode feedback circuits and a low power analog buffer capable of driving 50 Ω cable, maintaining sub-nanosecond rise time of the input. The ANUSPARSH-IIID ASIC has eight channels of fast leading edge discriminator with LVDS driver, a common threshold for all input channels and a multiplexed analog buffer, also capable of driving 50 Ω cable and maintaining sub-nanosecond rise time of the input. On the ANUSPARSH-III chipset based FE board, eight RPC pick-up strips are interfaced to two ANUSPARSH-IIIA ASICs and output of these ASICs have been interfaced to one ANUSPARSH-IIID ASIC. The test board of ANUSPARSH-III can accept both positive and negative inputs. This board is shown in Fig. 2. The LVDS output of ANUSPARSH-IIID ASIC is read through ANUPAL TDC ASIC based DAQ module [3] for measurement of RPC detector efficiency, noise rate and timing characteristics

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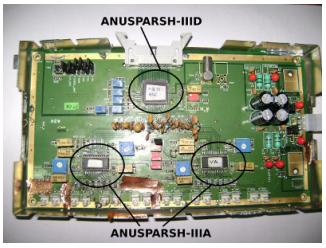


FIG. 2: The ANUSPARSH-III FE test Board.

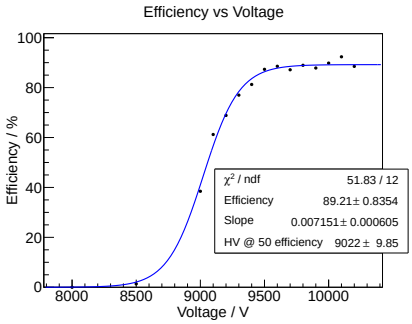
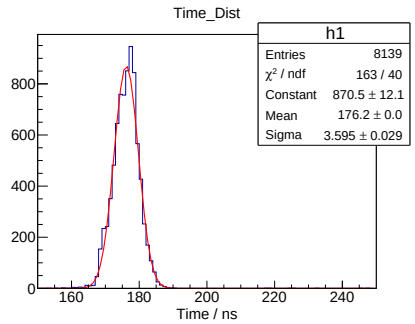
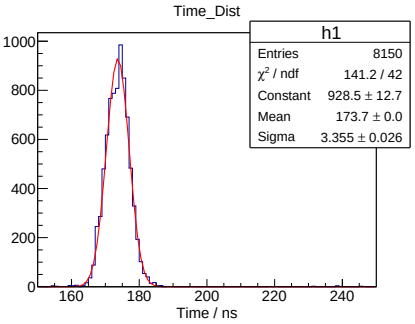


FIG. 3: Efficiency of RPC.



(a) Front Side



(b) Back Side

FIG. 4: Time distributions of the signals when paddle(i) was kept towards the front and back of the RPC.

from pick-up strips.

3. Trigger and setup

The trigger was generated by the telescopic coincidence of two paddles sandwiching the RPC: (i) Dimension - 40 × 18 × 1 cm^3, kept above, (ii) Dimension - 180 × 18 × 1 cm^3 which has PMT at both ends, kept below. The signal of paddle (ii) was the OR of the PMT signals at the two ends. Paddle(ii) is a part of the Hodoscope designed for characterization of RPCs. Paddle(i) was arranged in such a way so that it covered 5 strips in the RPC and was in line with paddle(ii). 5 strip signals were fed to the ANUSPARSH-III board. The discriminated signals were sent to the ANUPAL TDC ASIC based DAQ using 16 pin flat cable. The logical OR of the 5 strip signals were done in the DAQ.

4. Results

Efficiency vs. HV plot for the RPC when paddle(i) is kept towards the front of the RPC is shown in Fig. 3. Efficiency of ~ 90% is being observed for the RPC. The distribution of the time between the time of the trigger and the RPC strip signal is shown in Fig. 4 for the positive electrode of the RPC. Fig. 4(a) is when paddle(i) is kept towards the front of the RPC and Fig. 4(b) is when the paddle(i) is kept towards the back. The value of σ ~ 3.5 ns in both the cases. The value of σ is similar on the negative electrode side also.

5. Conclusions

Using the ANUSPARSH-III ASIC chipset based frontend, the RPC efficiency is measured to be ~90% and 'σ', the width of the distribution of time between the signal of the strips and the trigger is measured to be ~3.5 ns.

References

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[3] K. Hari Prasad, V. B. Chandratre et al, Design and development of portable DAQ system for RPC readout, DAE-BRNS NSNI, 2013.